**Memo: Current Status of Processor Milestone 3**

Section 1, Team 1a

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For this milestone, we changed the RTL and flipped it to have cycles be represented by rows. We adjusted it to look a lot more like the multicycle RTL we were presented in class. We adjusted the cells in the table so that the only empty cells were at the bottom, as well. In addition, we were able to remove a couple entire cycles from most instructions and one overall.

We changed how jumps and branches work. Jumps are supposed to be unconditional, but because all of our jumps are conditional, we combined branches and jumps to make two different types of jumps: jump to a label, and jump to a register. Branches were removed completely. We also needed a more accurate way to jump to labels, so we made jump label a 32 bit instruction to accommodate.

We modified our datapath to accommodate the new commands, and drew a new, neat version to scan.

Our group wrote tests for both components and the datapath. For these tests, we decided to write what kind of binary input there would be and what kind of binary output we would expect. Each component individually was tested, and each unique path through the datapath was tested.

We already had control signals implemented, and moved them out of the RTL and under a separate heading.